14.7 A 0.13µm CMOS SoC for All Format Blue and Red Laser DVD Front-end Digital Signal Processor

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A system on a chip (SoC) has been developed to be a front-end device for All Format DVD (AFDVD) systems. Transfer rates of up to 550Mb/s are achieved for 8× HD-DVD/BD, and DVD/CD reading and recording. Figure 14.7.1 depicts the SoC block diagram that consists of an analog front end (AFE), servo signal processing, partial response maximum likelihood (PRML) read channel, Disc Controller, and Servo System.

The PRML read channel is an asynchronous mixed signal path that transforms the optical channel data into a partial response pulse shape. This PRML is a PR(1,2,α,2,1) class, where α can be programmed as 2 or 2.5. Figure 14.7.2 shows the PRML channel, which includes an automatic gain and offset control, asymmetry correction, digital timing recovery and a speed tracking loop to ensure data detection for any constant or variable linear velocity modes such as CLV, CAV, ZCLV and PCAV.

The detected optical signal is applied as a differential voltage or current to the AFE with programmable input impedance (ZIN) from 50Ω to 2kΩ. A programmable attenuator adjusts the signal level by a coarse gain control. A variable gain amplifier (VGA) adjusts the signal to a desired fine target range. Therefore, wide input dynamic range is achieved while keeping the output signal within the dynamic range of the 7b ADC. The continuous time filter (CTF) is a 7th order Bessel filter that operates as a coarse equalizer. The cut-off frequency and boost is correlated with the read speed.

The adaptive gain and offset control block (AGOC) controls the gain of the VGA, ZIN, and offset cancellation DAC. Thus, gain and offset control loops have interaction with other control loops such as data rate tracking to exploit ADC dynamic range, which was not obtained in designs with an external RF chip as in [1]. The 7b ADC achieves a 6.2ENOB at a sampling rate of 560MHz for 150MHz input. The result is obtained after auto-calibration as shown in Fig. 14.7.3, in which static and dynamic offset of all 128 comparators are digitally calibrated in parallel. The calibration sequence is performed at power up and compensated for temperature variation.

The high frequency components of the recovered data are boosted by an adaptive pre-equalizer. The land-pit asymmetry correction (LPAC) is a new approach to compensate the intrinsic and written asymmetry of the RF signal for all DVD formats. Figure 14.7.4 shows the LPAC adaptive loop that adds a correction pulse to the edges of the incoming signal. Asymmetry correction starts with finding the mean level of incoming signals for 3T and 4T sequences in the signal mean detector (SMD), followed by an IIR filter to obtain virtual zero value. The mean value of the output signal is provided by the second SMD/IIR for asymmetry factor calculation. At each step, the sequencer compares the input samples with virtual zero, and decides to add or subtract the correction pulse exactly on the signal edges. The correction pulse is similar to the impulse response of the overall optical channel, AFE and pre-equalizer, which is hardwired in an interpolator register bank. The weight of the correction pulse is adjusted by the asymmetry factor multiplier.

An interpolated timing recovery (ITR) method is used for read clock extraction. It decimates the over-sampled incoming data stream based on the threshold that is determined by the media type and corresponding RLL encoding. An Adaptive FIR filter scales the ITR output samples to the expected PRML levels. This FIR has a 15 tap structure with an LMS adaptation algorithm.

The Viterbi detector has 8 states for (2,10) EFM/EFM+ codes, 10 states for (1,7) 17PP and (1,10) ETM codes. Due to possible isolated pairs of ones and zeros in addition to the data pattern in BD or HD-DVD formats, two more states are added. The RLL decoder demodulates the Viterbi output bit stream into payload bytes that are sent to the buffer manager and ECC for error correction. The ECC engine has a pipe-lined implementation that works on a block to calculate the syndrome while the other block is getting filled from the buffer.

The Buffer Manager provides an optimized data map for the burst transfer in an external data buffer. This block implements a circular buffer with programmable priority for data access. The buffer manager calculates the next address pointer automatically, and masks the part of data to be transferred to host side. All internal memory including cache and program memory is about 700Kb which saves die area and provides faster disc read operation compared to architectures with internal SRAM [2].

The recording operation proceeds by detecting the write clock from the wobble signal. The wobble data is extracted from photo detector signals and the sync pattern is demodulated. If the Target Search block detects the target address, the write state machine starts writing data on the correct location based on the sync signal. In the write operation, the Encoder converts both data and ECC symbols to specific channel bits based on the media type, and inserts the control and sync.

The servo AFE obtains DPD samples and digitized sensor signals by two sub-ranging ADCs while 6 DAC blocks provide servo control outputs to the internal pre-drivers. The servo controller consists of a microprocessor with extended DSP instructions, peripheral units, and dedicated control logic. These logic blocks include a Differential Phase Detector (DPD) module for tracking, Spindle module for speed count, run-out interrupt and Track Count module for track crossing. RF defect detection and Media Recognition are also included. The controller processor and servo DSP communicate commands and data via 1KB of shared internal SRAM. The dedicated servo processor ensures fast DSP and control operation with up to 200MHz system clock for high disc speed. This leaves the controller processor free for task management, buffer memory management, data flow control, and calculation intensive tasks such as content protection algorithms - data encryption/decryption implemented by firmware.

An at-speed test mode allows the controller to access channel quality measure, and to adjust the PRML blocks for optimum performance. In an internal loopback test, the PRBS pattern is injected to the Encoder, and then to the AFE, which gives an average BER of 1.561×10^{-5} at the Decoder output. The eye pattern in Fig. 14.7.5 represents the data path performance in system tests with the servo loops operating at 2× speed.

Acknowledgments:
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References:
[1] J.S. Pan et al., "A CMOS Multi-Format Read/write SoC for 7× Blu-ray/16× DVD/56× CD," *ISSCC Dig. of Tech. Papers*, pp. 572-573, Feb., 2005.
[2] G.S. Choi et al., "A 0.18µm CMOS Front-End Processor for Blu-ray Disc Recorder with an Adaptive PRML," *IEEE J. Solid-State Circuits,* vol. 40, no. 1, pp. 342-350, Jan., 2005.
[3] K. Okamoto et al., "A Fully Integrated 0.13-µm CMOS Mixed-Signal SoC for DVD Player Applications," *IEEE J. Solid-State Circuits,* vol. 38, no. 11, pp. 1981-1991, Nov., 2003.

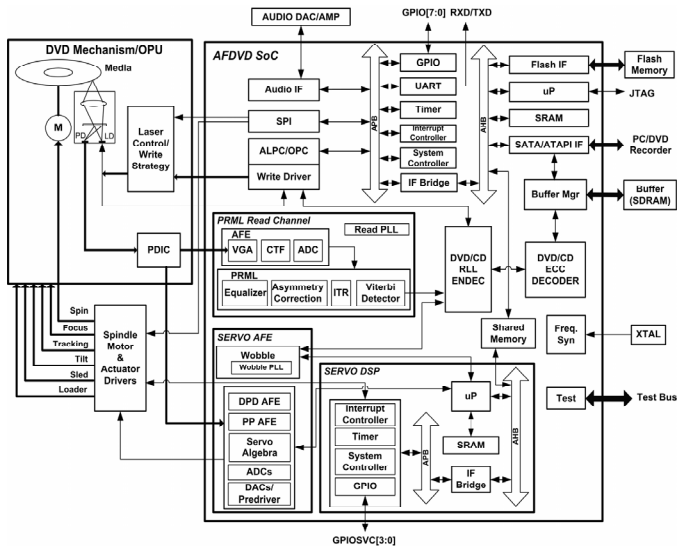

Figure 14.7.1: All format DVD SoC block diagram.

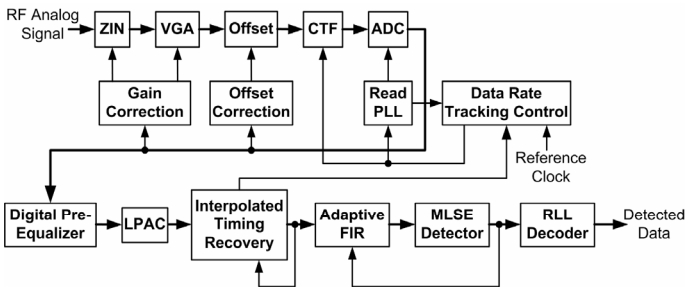

Figure 14.7.2: The PRML read channel structure.

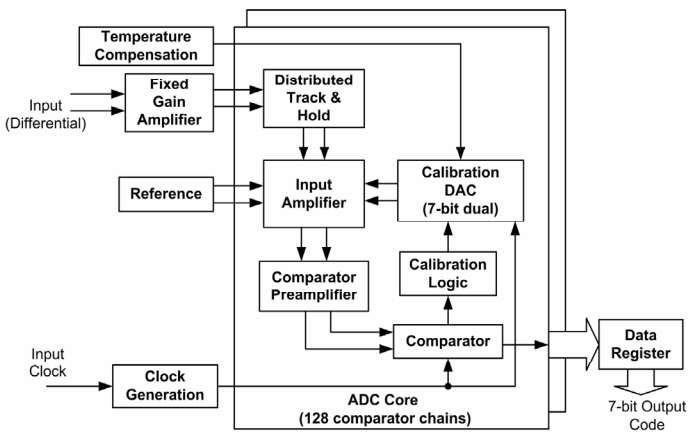

Figure 14.7.3: Read channel flash ADC block diagram.

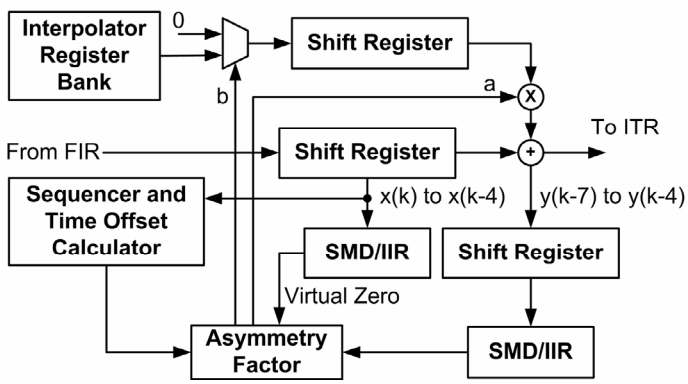

Figure 14.7.4: Asymmetry correction block diagram.

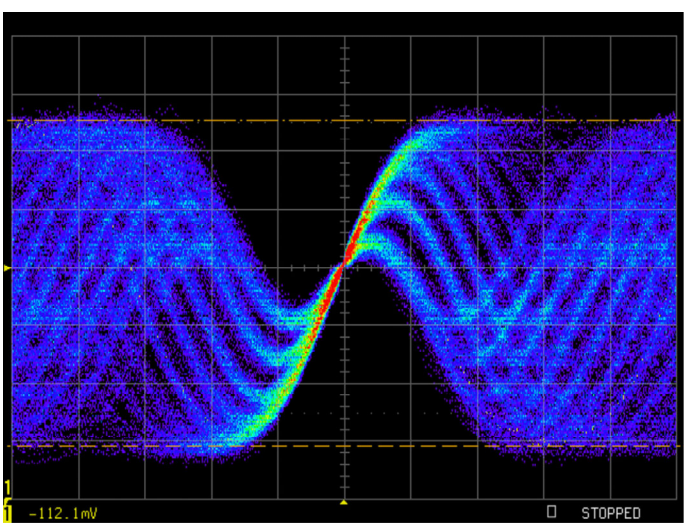

Figure 14.7.5: Eye diagram in 2× speed system test.

Package	TEPBGA 300 balls
Process Technology	0.13um 1-poly 7-metal CMOS
Supply Voltage	1.5V (digital core, analog) 3.3V (digital I/O, analog)
Die Size	7.748mm x 8mm = 62mm^2
Memory	24kB SRAM servo code 8kB SRAM servo data 16kB SRAM controller
Core Functions	PRML (7b ADC, Read PLL, equalizer, Viterbi Detector, Asymmetry Correction) RF and servo signal analog front end and processing Multi Format RLL Endec for Red and Blue laser ECC ARM946ES for controller Servo (ARM946ES, 10b ADC, 8b and 10b DACs, Wobble PLL) ALPC to support OPC/ROPC SRAM
No. of Transistors	640k Analog front end
No. of Gates	2.3 Million
Power Consumption	2.75 W for 2x blue laser playback (including RF and servo AFE)
Playback/Recording	DVD-ROM 16x DVD±R 16x/16x DVD±RW 16x/8x Blue laser DVD 8x/5x CD-ROM 52x CD-R 52x/52x CD-RW 52x/48x

Figure 14.7.6: All format DVD SoC characteristics.

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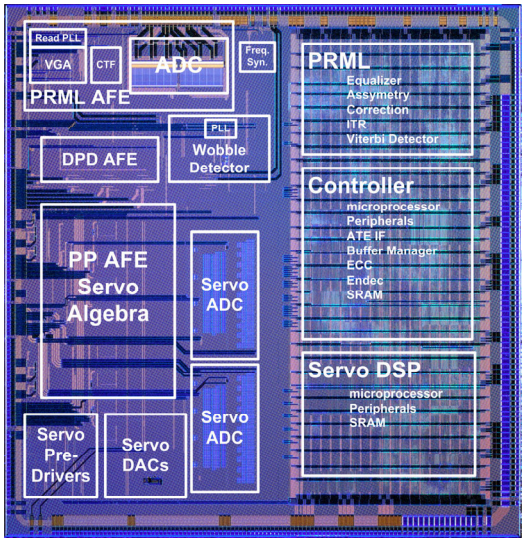

Figure 14.7.7: Chip micrograph.

